WHAT IS CLAIMED IS:

1. A sample assembly for a thermoelectric analyzer comprising:

(a) an electrically-insulating substrate;

(b) a pair of junction electrode layers formed on said substrate;

(c) a sample fixed to said substrate;

(d) an adhesive layer disposed between said sample and said substrate and made of a material selected from a group consisting of indium and gold-tin alloy;

(e) a pair of electrode layers formed on a same plane of said sample; and

(f) two electrically-conductive wire means: one electrically-conductive wire means connecting one of said electrode layers with one of said junction electrode layers, and another electrically-conductive wire means connecting the other of said electrode layers with the other of said junction electrode layers.

2. A sample assembly according to claim 1, wherein said adhesive layer is made of indium.

3. A sample assembly according to claim 2, wherein said substrate is made of a material selected from a group consisting of aluminum nitride, boron nitride, beryllium oxide and aluminum oxide.

4. A sample assembly according to claim 3, wherein each of said

electrode layers and said junction electrode layers is made of a multilayer including a top layer which is a gold layer, and said wire means are gold wires.

5. A sample assembly according to claim 4, wherein said pair of electrode layers, said pair of junction electrode layers and said wire means are arranged mirror-symmetrical with respect to a center of said sample.

6. A sample assembly according to claim 5, wherein said sample is compound semiconductor.

7. A sample assembly according to claim 1, said adhesive layer is made of gold-tin alloy.

8. A sample assembly according to claim 1, wherein said substrate is made of a material selected from a group consisting of aluminum nitride, boron nitride, beryllium oxide and aluminum oxide.

9. A sample assembly according to claim 1, wherein said sample assembly is adapted to be supported by two support rods which serve also as conductors for an electric circuit and gold washers are inserted between said support rods and said junction electrode layers.

10. A sample assembly according to claim 1, wherein each of said

electrode layers and said junction electrode layers is made of a multilayer including a top layer which is a gold layer, and said wire means are gold wires.

11. A sample assembly according to claim 1, wherein said pair of electrode layers, said pair of junction electrode layers and said wire means are arranged mirror-symmetrical with respect to a center of said sample.

12. A sample assembly according to claim 1, wherein said sample is compound semiconductor.

13. A sample assembly according to claim 1, wherein said sample has a plane size of 5 mm × 5 mm or less.